What is claimed is:

1. A floating point accumulator circuit comprising:

an exponent path; and

a mantissa path having an output node fedback to an input node, and at least one sequential element in an internal data path.

2. The floating point accumulator circuit of claim 1 wherein the exponent path includes a comparator to compare three bit exponents of two floating point numbers, and the mantissa path includes a constant shifter in the internal data path to conditionally shift a mantissa of one of the two floating point numbers by thirty-two bits.

3. The floating point accumulator circuit of claim 2 wherein the mantissa path further includes:

an adder circuit to add mantissas of the two floating point numbers; and

a multiplexor in parallel with the adder to conditionally select one of the mantissas to be a resultant mantissa.

4. The floating point accumulator circuit of claim 1 wherein the mantissa path further includes an adder path and a bypass path, the adder path including an adder circuit, and the bypass path not including an adder circuit.

5. The floating point accumulator circuit of claim 4 wherein the mantissa path further includes a partial normalization path.

6. The floating point accumulation circuit of claim 5 wherein the adder path, bypass path, and partial normalization path each include at least one intermediate register.

7. The floating point accumulator circuit of claim 4 wherein the adder circuit is configured to sum numbers in carry-save format.

8. An integrated circuit comprising:

a multiplier coupled to receive operands and to produce a product; and

a multi-threaded accumulator coupled to the multiplier to receive the product.

9. The integrated circuit of claim 8 further comprising a control circuit to interleave input operands from different operand streams into the multiplier.

10. The integrated circuit of claim 8 wherein the multi-threaded accumulator is configured to sum floating point numbers having mantissas in carry-save format.

11. The integrated circuit of claim 10 wherein the multi-threaded accumulator includes at least one intermediate register to facilitate accumulating two interleaved product streams simultaneously.

12. The integrated circuit of claim 8 further comprising a floating point conversion unit coupled between the multiplier and the multi-threaded accumulator to convert the product from a first floating point representation to a second floating point representation.

13. The integrated circuit of claim 12 wherein the first floating point representation includes an exponent field having a least significant bit weight of one, and the second floating point representation includes an exponent field having a least significant bit weight of thirty-two.

14. The integrated circuit of claim 13 wherein the multi-threaded accumulator circuit includes at least one constant shifter to conditionally shift a mantissa thirty-two bit positions.

15. The integrated circuit of claim 8 wherein the integrated circuit is a circuit selected from the group comprising a processor, a memory, a memory controller, an application specific integrated circuit, and a communications device.

16. An accumulator circuit to accept operands from different threads interleaved in time, the accumulator having intermediate registers to simultaneously hold partial results from each of the different threads.

17. The accumulator circuit of claim 16 further comprising:
a constant shifter prior to a first intermediate register; and
a multiplexor subsequent to the first intermediate register.

18. The accumulator circuit of claim 17 further comprising:
an adder circuit prior to a second intermediate register; and
a second multiplexor subsequent to the second intermediate register.

19. The accumulator circuit of claim 16 wherein the operands are floating point numbers in IEEE single precision format.

20. The accumulator circuit of claim 16 wherein the operands are floating point numbers in a floating point format other than IEEE single precision format.

21. The accumulator circuit of claim 16 wherein the floating point numbers include exponent fields with a least significant bit weight other than one.

22. The accumulator circuit of claim 21 wherein the floating point numbers include exponent fields with a least significant bit weight equal to thirty-two.

23. A multi-threaded floating point multiply-accumulator circuit comprising:

a multiplier to produce a product; and

an accumulator coupled to receive the product from the multiplier, the accumulator including sequential elements to provide a multi-threaded capability.

24. The multi-threaded floating point multiply-accumulator circuit of claim 23 further comprising a floating point conversion unit to convert the product from a first exponent weight to a converted product with a second exponent weight.

25. The multi-threaded floating point multiply-accumulator circuit of claim 24 wherein the accumulator is configured to produce a present sum from the converted product and a previous sum having the second exponent weight.

26. The multi-threaded floating point multiply-accumulator circuit of claim 25 further comprising a post-normalization unit to convert the present sum to a floating point resultant having the first exponent weight.

27. The multi-threaded floating point multiply-accumulator circuit of claim 23 wherein the accumulator includes:

an adder path; and

an adder bypass path.

28. The multi-threaded floating point multiply-accumulator circuit of claim 27 wherein the multiplier is configured to produce a product with an exponent weight of one.

29. The multi-threaded floating point multiply-accumulator circuit of claim 28 further comprising a floating point conversion unit to convert the product from an exponent weight of one to an exponent weight of thirty-two.

30. The multi-threaded floating point multiply-accumulator circuit of claim 29 wherein the accumulator is configured to accumulate numbers in carry-save format.